

CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters PATENT is:

1. A method of forming a poly-poly capacitor, a MOS transistor, and a bipolar transistor simultaneously on a substrate comprising the steps of:

depositing and patterning a first layer of polysilicon on the substrate to form a first plate electrode of said capacitor and on an electrode of the MOS transistor; and

depositing and patterning a second layer of polysilicon on the substrate to form a second plate electrode of said capacitor and an electrode of the bipolar transistor,

said second layer of polysilicon comprising SiGe polysilicon.

2. The method of Claim 1 wherein electrode of the MOS transistor comprises a polysilicon gate formed on a gate oxide, said gate oxide being formed on a surface of the substrate, the substrate having source and drain regions beneath said polysilicon gate.

1 3. The method of Claim 2 wherein the substrate is a
2 semiconducting material selected from the group
3 consisting of Si, Ge, SiGe, GaAs, InAs and layered
4 semiconductor substrates.

1 4. The method of Claim 2 wherein the substrate further
2 comprises shallow trench isolation regions and a
3 subcollector region, said subcollector region being
4 formed between said shallow trench isolation regions.

1 5. A method of forming a poly-poly capacitor comprising
2 the steps of:

3 (a) forming a film stack on a surface of a semiconductor
4 structure, said structure comprising at least a gate
5 region of a metal oxide semiconductor device and a bottom
6 polysilicon plate of a poly-poly capacitor formed on a
7 surface thereof, said film stack including at least a
8 polysilicon layer;

9 (b) forming a bipolar opening in said film stack
10 exposing at least a portion of said surface of said
11 semiconductor structure, wherein said bipolar opening is
12 formed in a region in which a bipolar device will be
13 subsequently fabricated;

14 (c) simultaneously forming a SiGe epi layer in said
15 bipolar opening, while forming a SiGe polysilicon film on
16 exposed portions of said polysilicon layer of said film
17 stack;

18 (d) selectively doping portions of said SiGe polysilicon
19 film as well as said SiGe epi layer with a dopant atom of
20 a first conductivity type;

21 (e) forming a patterned passivating layer on a portion
22 of said doped SiGe epi layer;

23 (f) forming a patterned doped emitter polysilicon layer
24 on said patterned passivating layer as well as on said
25 doped SiGe epi layer formed in said bipolar opening
26 thereby completing fabrication of said bipolar device,
27 said doped emitter polysilicon layer having a different
28 conductivity than said doped SiGe epi layer; and

29 (g) removing selective portions of said doped SiGe
30 polysilicon film and remaining layers of said film stack
31 so as to expose said gate of said metal oxide
32 semiconductor while protecting said bipolar device region
33 and said doped SiGe polysilicon layer overlying said
34 bottom polysilicon plate of said poly-poly capacitor.

35 6. The method of Claim 5 wherein said film stack further
36 comprises a bottom insulator layer and an optional top
37 insulator layer.

1 7. The method of Claim 6 wherein said top and bottom
2 insulator layers of said film stack are the same or
3 different insulative materials selected from the group
4 consisting of SiO_2 and Si oxynitrides.

1 8. The method of Claim 7 wherein said top and bottom
2 insulator layers are both composed of SiO_2 .

1 9. The method of Claim 6 wherein said top insulator
2 layer has a thickness of from about 100 to about 1000 Å.

1 10. The method of Claim 6 wherein said bottom insulator
2 layer has a thickness of from about 50 to about 1000 Å.

1 11. The method of Claim 5 wherein said polysilicon layer
2 has a thickness of from about 100 to about 1000 Å.

1 12. The method of Claim 5 wherein said bipolar opening
2 is formed by employing lithography and etching.

1 13. The method of Claim 12 wherein said etching is
2 carried out by reactive-ion etching or ion beam etching.

1 14. The method of Claim 6 wherein said optional top
2 insulator layer is removed utilizing an etch process that
3 is highly selective in removing said top insulator layer
4 as compared to said underlying polysilicon layer.

1 15. The method of Claim 5 wherein said SiGe epi layer
2 and said SiGe polysilicon film are formed simultaneously
3 utilizing a deposition process that is carried out at
4 temperatures of from about 900°C or below.

1 16. The method of Claim 15 wherein said temperature of
2 said deposition process is from about 400° to about
3 500°C.

1 17. The method of Claim 5 wherein said SiGe epi layer
2 and said SiGe polysilicon film have the same or different
3 thickness.

1 18. The method of Claim 17 wherein said SiGe epi layer
2 and said SiGe polysilicon film have the same thickness,
3 said thickness of each layer being of from about 1000 to
4 about 5000 Å.

1 19. The method of Claim 5 wherein said dopant used in
2 doping said SiGe epi layer is boron having a
3 concentration of about 4×10^{15} atoms/cm².

1 20. The method of Claim 5 wherein said dopant used in
2 doping said emitter polysilicon is As.

1 21. The method of Claim 5 wherein said patterned emitter
2 doped polysilicon layer is formed by depositing a layer
3 of polysilicon, doping said layer with a dopant and
4 thereafter subjecting said emitter doped polysilicon
5 layer to lithography and etching.

1 22. The method of Claim 1 wherein optional spacers are
2 formed on said poly-poly capacitor.

1 23. The method of Claim 22 wherein said optional spacers
2 are formed by deposition, lithography and etching.

1 24. A poly-poly capacitor comprising two plate
2 electrodes, wherein at least one of said plate electrodes
3 is composed of SiGe polysilicon, said plate electrodes
4 being separated by an insulator structure.

1 25. The poly-poly capacitor of Claim 24 wherein one of
2 said plate electrodes is composed of polysilicon and the
3 other plate electrode is composed of SiGe polysilicon.

1 26. The poly-poly capacitor of Claim 24 wherein both of
2 said plate electrodes are composed of SiGe polysilicon.

1 27. The poly-poly capacitor of Claim 24 wherein at least
2 one said plate electrodes is polysilicon from a FET gate
3 or a bipolar emitter.

1 28. The poly-poly capacitor of Claim 24 further
2 including a bipolar device region and a FET region,
3 wherein said capacitor, bipolar device region and FET
4 region are electrically isolated from each by isolation
5 regions.

1 29. A semiconductor device, comprising

2 a capacitor having first and second plate electrodes, one
3 of said plate electrodes being comprised of a first
4 conductive patterned layer; and

5 a bipolar device having first and second electrodes, one
6 of said electrodes being comprised of said first
7 conductive patterned layer;

wherein said first conductive patterned layer is comprised of SiGe material.

30. A semiconductor structure, comprising

a first layer of polysilicon patterned to form a first electrode of a MOS device and a first plate electrode of a capacitor, and

a second layer of SiGe/polysilicon patterned to form a first electrode of a bipolar device and a second plate electrode of said capacitor,

said second layer being comprised of SiGe polysilicon.